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ABSTRACT

This paper addresses the integrated circuit industry needs for non-isothermal simulation in device reliability analysis, initial input factor sensitivity analysis and their software implementation. The key reliability issues are the hot-electron induced oxide damages and electro-static discharge (ESD) damages. The main purpose of this work is to provide a design aid tool to improve device reliability and performance. The reliability simulator developed in this work not only predicts designed device reliability, but also provides some information about the effect of manufacturing variations on reliability. This is accomplished by combining the statistical methodology with existing technology computer aided design (TCAD) tools. The design of experiment (DoE) technique can be successfully employed to analyze the effect of manufacturing variations on the SOI device reliability. As an example, the reliability analysis and the statistical analysis have performed on SOI MOS devices (partially depleted and fully depleted SOI) and submicron bulk-Si MOSFET's to verify the applied modeling method.

Keywords: reliability, hot-electron effect, electrostatic discharge, STADIUM SOI.

1. INTRODUCTION

With the continuous down scaling of the device dimensions and the emergence of the advanced material technology such as silicon-on-insulator(SOI) in ULSI circuit, the reliability has become a more important concern than in the past. One of the key reliability issues is the hot-carrier induced oxide damages which result in the device degradations The hot-electron induced device degradation is a long-term process. In the conventional computer-aided design approach, physical aging of integrated circuit elements due to degradation mechanisms has been a secondary concern and qualification of circuit reliability has been accomplished by burn-in tests after manufacturing. This approach, the repetition of "design-manufacturing-test" cycle is probably expensive and does not optimize the device reliability and circuit performance.

Another important reliability issue is electro-static discharge (ESD) performance of non-isothermal devices. ESD induced device failure is the thermally destructive process. Various models such as the human body model(HBM), the charged device model(CDM), and the machine model(MM) have been developed to simulate the electrostatic discharge event [1]. ESD event can cause direct, indirect, or latent damages in the semiconductor devices. A latent failure as a result of earlier exposure to electrostatic discharge is not an immediately detectable problem but a time-dependent malfunction. Many researchers have reported the evidence to support the presences of latency effects [2][3]. However the cumulative effect of repeated discharges is not well characterized.

Silicon-on-insulator(SOI) MOSFET has emerged a leading candidate to replace bulk-silicon MOS for ULSI application.The silicon-on-insulator device has many advantages over its bulk counterpart. However, some fundamental problems of SOI technology such as self-heating, poor ESD susceptibility and kink effects due to floating body are also present. In the past, non-isothermal simulation was particularly important for power device. However, the electrical characteristics of modern ULSI device structures may be significantly altered by electro-thermal effect.This is seen in submicron MOSFET structures and the self-heating effect is even more pronounced in SOI MOSFET's due to the low thermal conductivity of the buried oxide layer. Since local self-heating has turned out to be a crucial effect in the device operation, nonisothermal condition should be considered in device modeling and the reliability analysis [4].

Optimization of circuit performance and reliability is one of the major concerns in circuit design. ESD protection circuits and CMOS SOI circuits are built on the same SOI wafer and high performance and good reliability should be realized. This is very difficult to achieve by pure SOI technology alone. The development of reliable SOI circuits requires a characterization of the important process and design-related parameters for hot-electron induced degradation and ESD behavior. These parameters

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have been determined experimentally using test structures with process and design variations. This does not optimize the device reliability and circuit performance. Moreover, some process and design parameters have adverse effects on device performance or reliability. The lightly doped drain (LDD) process, for example, has been employed to improve hot-carrier reliability, but this technology significantly degrades ESD performance [5][6][7]. Therefore, we need to develop an understanding of device reliability and performance based on layout geometries and process input parameters.

With the growing importance of CMOS technologies, accurate analysis of the effect of manufacturing variations on device performance has become an important issue in modern ULSI IC's. As the size of device geometries is reduced into submicron, small perturbations inherent to manufacturing play more important role than in the past. The device variations due to the naturally occurring process variations of the manufacturing line may result in circuit performance and reliability degradation and low product yields. The statistical methodology should be introduced to analyze initial input factor effects on device performance and reliability. The development and use of accurate reliability simulation tools which have statistical analysis functions are therefore essential to improve reliability. The statistical analysis tool, STADIUM SOI/Reliability Simulator, has been developed at Florida Tech.[8][9]. The methodology used in STADIUM SOI/Reliability simulator is to make IC's with predictable high reliability not by measuring the output at the end of production, but by controlling the process input factors that impact the product performance or reliability.

2. THE PROGRAM STADIUM SOI/RELIABILITY

The proposed reliability simulator has been developed to be a partner of STADIUM SOI. STADIUM SOI has been developed for the statistical analysis of target responses which are usually the device characteristics or circuit performances. Because of the importance of reliability in the modern integrate circuit, the reliability analysis module is implemented in STADIUM SOI. These programs are written in C and X-View programming language and implemented on the X-window environment. The experiments are set up with the user inputs which are translated in a window interface module and simulations are carried out. Based on simulation results, statistical analyses are performed and the results are provided to the user. A easy-to-use graphical user interface helps an inexperience engineer to develop information with minimum complexity. The overall scheme of STADIUM SOI/Reliability simulator is shown in Figure 1.

The simulator can be used in two ways, reliability test mode and statistical analysis mode as shown in Figure 2. In the reliability test mode, the reliability simulator works independently with STADIUM SOI. The simulator predicts the designed device

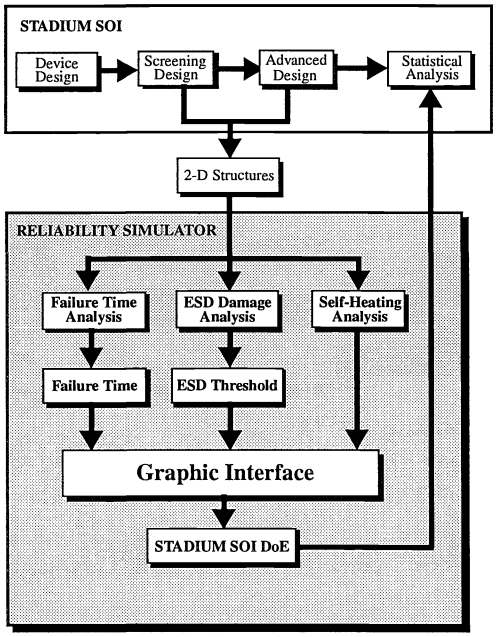

Fig. 1. STADIUM SOI/Reliability Simulator

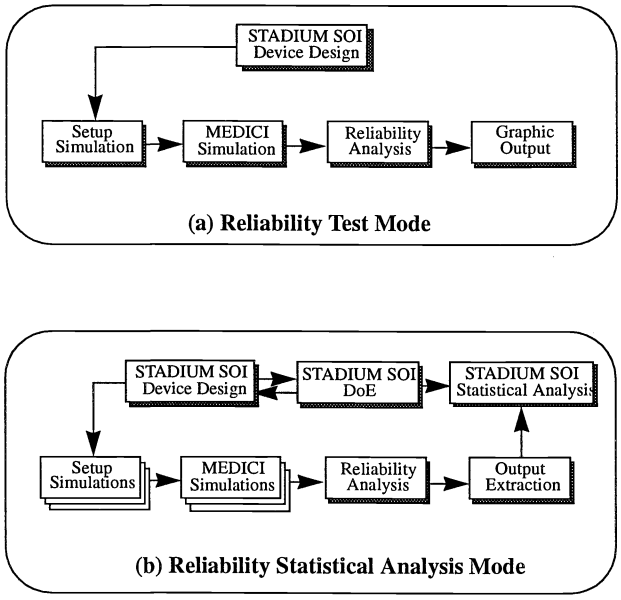

Fig. 2. Flow Diagram of Reliability Analysis Modes

reliability such as hot-carrier induced failure time analysis and ESD performance. The results are provided graphically. In the statistical analysis mode, the statistical analysis module of STADIUM SOI is involved to analyze the manufacturing variation effects on the device reliability. The design of experiment(DoE) technique is employed for the statistical analysis[10]. The statistical analysis leads to the development of regression models which are used to compute estimated means and variances of significant response variables, thereby ultimately enabling substantially improved yield and performance prediction.

The failure time due to hot-electron degradation and ESD performance are considered to be the target responses to be analyzed. The accurate analysis of reliability demands a deep understanding of degradation mechanisms, precise simulations and correct interpretation. The proposed reliability simulator accommodates these requirements. For the better statistical analysis results, the accurate estimation of target response values should be obtained. One of the reliable means of estimating the device characteristics and circuit performance is using the 2-D computer simulation programs. For this reason, the commercial numerical simulation program and the statistical methodologies have been employed in STADIUM SOI/Reliability simulator.

For the modeling of the device reliability, a great deal of experience and time is required to setup simulation and interpret the simulation results. The development of the reliability simulator significantly reduce this complexity. STADIUM SOI/Reliability simulator automatically perform the tasks such as setup simulation, data extraction, interpolation data and estimation target values. The STADIUM SOI/Reliability Simulator has the five functional modules as shown in Figure 3. Each module performs the following task;

- Process Flow Design Module: help an user to develop the process.
- Simulation Control Module (Design of Experiment Module): setup experiments for the statistical analysis.
- Simulation Output Module: provide graphic information to examine the generated device structures
- Statistical Analysis Module: Perform the input factor sensitivity analysis on target responses
- Reliability Analysis Module: analyze the designed device reliability (device failure time and ESD threshold voltage)

Figure 4 shows the flow diagram of simulation. With the structures generated by the DoE controlled process simulations, the device simulations are carried out and the target values are calculated by the post processing in the reliability simulator. The extracted target responses such as the device failure time or ESD threshold voltages are sent to the STADIUM SOI library directory and used in the statistical analysis.

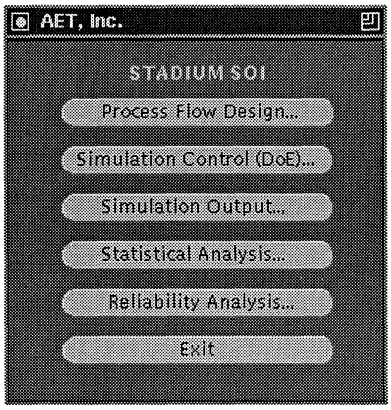

Fig. 3. STADIUM SOI/Reliability Main Window

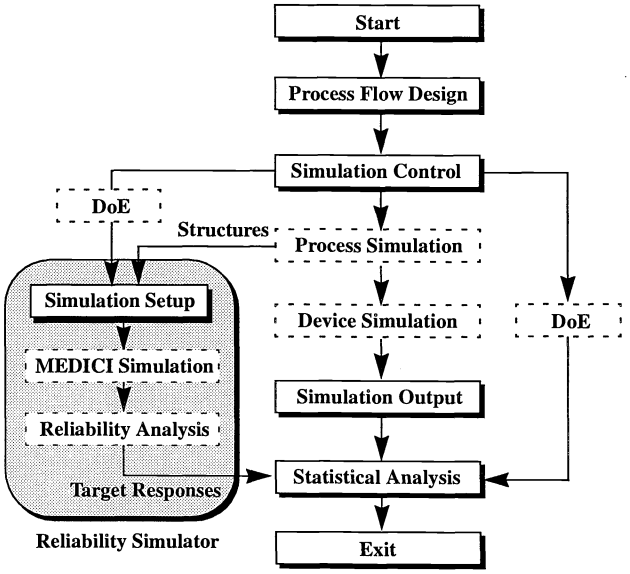

Fig. 4. STADIUM SOI/Reliability Flow Diagram

2.1. FAILURE TIME ANAYSIS MODULE

The inherently high electric fields present in short channel MOSFET's can lead to reliability problems. One particular problem is concern with hot electrons that are injected from the channel into the gate. Degradation of the device occurs as a fraction of the interface traps in the gate oxide which are created by hot electrons. The physics of the channel hot-electron injection is well understood [11][12]. STADIUM SOI/Reliability provides a easy-to-use user interface window for the failure time analysis. The main function of this window is to set up simulations. The menu items such as bias condition, degradation item, device width, simulation method, stress type and bias condition can be specified in this window. If these values are not given by an user, STADIUM SOI/Reliability provides the default values which are considered optimum for simulation.

The hot-electron induced oxide damages result in the device degradation such as the threshold shift, transconductance reduction and drain current degradation. An user can specify the degradation item and its value by using the failure time analysis window(i.e. 10% of threshold voltage may cause the device failure). Various approaches have been made previously for monitoring the hot-carrier related degradation in MOS transistors. The substrate current is a good predictor to monitor the device degradation. Since no current flows into the substrate in SOI device due to buried oxide layer, the impact ionization current is used in the proposed simulator as a means of predicting for the device failure time in the proposed simulator.

Two stress types, DC stress and AC pulse stress (also called static stress and dynamic stress) are employed in the analysis as shown in Figure 5 and Figure 6. If DC stress condition is chosen, the gate and drain bias electrode can be specified. The user specified bias conditions are directly applied the designed device structure as shown in Figure 5. If the AC bias condition is selected, the AC bias condition items, power supply voltage specification, simulation method should be specified. For the AC pulse test simulation, the conventional CMOS inverter circuit as shown in Figure 6 is used. The CMOS inverter circuit consists of an NMOS and an PMOS and the device under test can be either a n-channel MOS or a p-channel MOS. If the NMOS is selected as the test device, the PMOS is defined to the dummy device in the CMOS circuit. (For the simulation purpose this device called "dummy" should be defined. This device is Spice model and the MOS parameter is given by an user or by the simulator as a default value). Contrarily, if the PMOS is chosen as the test device, the NMOS will be the dummy device.

Two simulation methods are proposed in the failure time simulator, "One Step" method and "Repetitive" method. The one step method is employed to save simulation time. This method is based on the assumption that the inverter voltage waveform is not changed for the simulation period. This is usually not true because the voltage waveform is actually changed during the operation due to the device aging. The repetitive simulation method is adopted to overcome the above deficiency. The evolution of hot-electron related damage in the device is automatically simulated at predetermined time intervals, instead of extrapolating the long-term degradation by using only the initial simulation results. The repetitive simulation scheme ensures the accurate prediction of the degradation process.

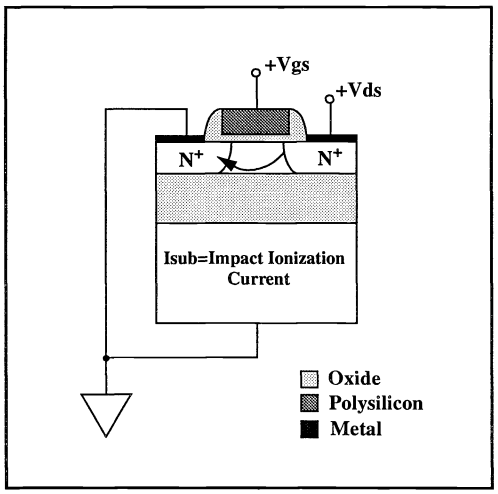

Fig. 5. DC Failure Time Simulation Scheme

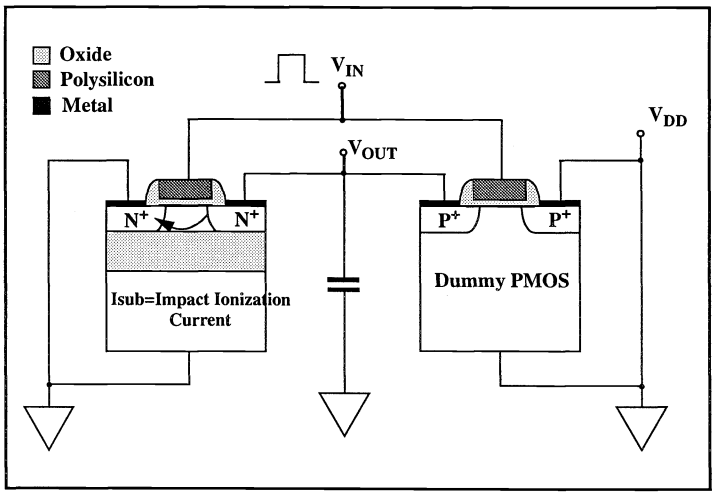

Fig. 6. AC Failure Time Simulation Scheme

2.2. ELECTROSTATIC DISCHARGE FAILURE MODULE

The device failure under electrostatic discharge(ESD) is thermally originated mechanism. The temperature inside the filament increases due to joule heating and eventually thermal runaway occurs with the destructive failure of the device. After the ESD stress, the molten region recrystallizes and a low-resistance filament is formed in the high resistance depletion region. This filament may cause junction leakage at even low applied voltage. For this reason, the silicon melting temperature is considered as a good estimator for ESD induced failure of the semiconductor device. The conditions for thermal breakdown can be determined from a solution of the heat flow equation. The ESD threshold voltage was interpreted as the applied ESD stress voltage at which the lattice temperature of the device reached the silicon melting temperature. In a small dimension device, there is less space available for heat dissipation and this may increase lattice temperature significantly. The the buried oxide layer in the SOI device accelerates lattice temperature rising and results in poor ESD performance.

ESD failure analysis module is implemented to set up conditions for the electro-thermal simulation. By using the main window, the simulation conditions such as ESD stress conditions, device type and device width can be set up. The software runs electron-thermal simulation with user defined ESD stress values. The simulator automatically selects the next ESD stress values for the simulation based on the first simulation results and the simulations are run again. After all necessary simulations are performed, the interpolation module is used to calculate the ESD threshold voltage at which the device lattice temperature reaches the silicon melting point ($1412°C$). The impact ionization effect can be included in simulation by turning on the "Impact Ionization" model in the menu. This effect is important because the impact ionization has strong cooling effect on the lattice temperature. For the ESD analysis of nonisothermal devices, it is recommended to include the impact ionization model in the simulation.

For the ESD simulation, the equivalent circuit is directly connected to the device under test and the transient circuit simulations were performed by using MEDICI simulator. Three different ESD models, human body model(HBM), charged device model(CDM) and machine model(MM) are applied to the test device. The equivalent circuit model and their discharge current are shown Figure 7 and Figure 8. The equivalent circuits are identical but the circuit element values are different for the ESD stress models as shown in Figure 7. These values are provided by the ESD simulator and can be modified by an user.

The thermal resistance default value is given by the ESD simulator. The thermal resistance is important for two reasons. First, the actual device is much deeper than the simulation structure, thus the thermal resistance should be specified to produce the accurate results of electro-thermal simulation. Second, the thermal resistance is also affected by the device package type. Since the thermal runaway of heat inside device can be different by using a different package, this also can have an effect on the ESD performance. The default value is also given by the simulator.

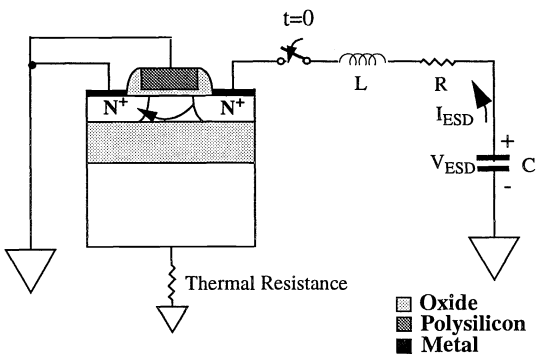

Fig. 7. Equivalent Circuit for ESD Simulation (HBM: C=100pF, L=7.5uH, R=1.5kohm, CDM: C=10pF, L=50nH, R=1ohm, MM: C=200pF, L=1.0uH, R=10ohm)

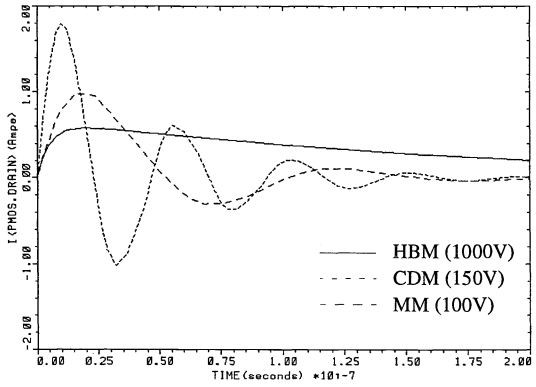

Fig. 8. Discharge current for the different ESD Model

3. EXAMPLE A: RELIABILITY SIMULATION RESULTS

The reliability analysis have been performed on SOI MOS devices (partially depleted and fully depleted SOI) and bulk-silicon MOS to verify the applied modeling method. The simulations are carried out on the two dimensional device simulator TMA MEDICI, based on device geometry and doping profile generated by TMA SUPREM4 process simulator. Table 1 shows the geometry and electrical characteristics of the device used for simulations.

For the failure time test, DC bias conditions with the gate bias voltage (1.5V) and the drain voltage (3.0V) were chosen so that the maximum degradation occurred. The impact ionization current was extracted and used as substrate current in the analysis. Both isothermal and non-isothermal conditions were applied to the simulations. The temperature dependent models for diffusion, mobility and impact ionization were included in the non-isothermal simulation and alternatively, local electric field dependent models were used in the isothermal simulation. For the ESD simulation, the equivalent circuit is directly connected to the device under test and the transient circuit simulations were performed by using MEDICI simulator. Three different ESD models, human body model(HBM), charged device model(CDM) and machine model(MM) are applied to the test device.We have investigated the effect design parameters on the overall SOI and bulk-Si MOS reliability.

Figure 9 shows both isothermal and non-isothermal failure time simulation results as a function of device channel length. The self-heating effect for the FD and PD SOI MOS is critical. Without including the electro-thermal effect in the simulation, the failure time is considerably underestimated due to the higher mobility at the lower temperature. Contrarily, the rapid thermal runaway occurs through the silicon substrate in the bulk silicon device. As silicon film thickness increases, the device failure time is slightly decreases in the FD SOI in some degree but it is not seen in PD SOI MOS as shown in Figure 10. It is clear that the device failure time is affected by the self-heating but not by the silicon film thickness variation.

Figure 11 and Figure 13 show the ESD failure voltage for human body model(HBM), machine model(MM) and charged device model(CDM) stress condition as a function of silicon film thickness. More enhanced ESD performance with increasing silicon film thickness has been shown in fully depleted SOI devices for all stress model. In SOI technologies, large-area vertical PN junctions are not available and the ESD discharge current path is restricted to the thin silicon film. For the same power dissipated in the transistor, the silicon temperature increases with decreasing silicon film thickness because of the reduction of heat transfer capacity in the smaller silicon volume. As a result, the ESD performance will be worse as the silicon thickness is scale down.

By increasing the channel width of the device, ESD performance improves accordingly as shown in Figure 12. However, the ESD threshold voltage of the SOI device does not increase as much as that of the bulk silicon device. Good ESD protection can not be obtained by simply enlarging the device width as is routinely done for ESD protection.

The ESD performance can improve as the gate-to-contact spacing increases. This is not seen in the SOI MOSFET's as shown in Figure 14. It is due to the presence of an insulating buried oxide. The heat generated in a SOI MOSFET can only flow later-

Table 1: Architectures and Device Characteristics for Four Different Technology Devices

Device Architectures	**Technology**				
	FD SOI	**PD SOI**	**NMOS1**	**NMOS2**	**Units**
Effective Channel Length	0.13	0.14	0.21	**0.22**	microns
Gate Oxide Thickness	9.0	9.0	6.5	9.6	nm
Lightly Doped Drain	none	none	yes	yes	-
S/D Junction Depth	0.075	0.15	0.28	0.21	microns
Epitaxial layer Thickness	none	none	2.0	3.0	microns
Silicon Film Thickness	0.075	0.15	none	none	microns
Buried Oxide layer Thickness	0.38	0.38	none	none	microns
Device Characteristics					
Threshold Voltage (Vth)	0.2	0.25	0.73	0.68	V
Transconductance (Gm)	8.7E-5	7.9E-5	6.4E-5	5.7E-5	A/um-V
Subthreshold Slope (SS)	68.0	76.3	78.2	89.3	mV/dec
Breakdown Voltage (BV)	4.5	5.2	6.8	7.2	V

ally, resulting in the same temperature through the active layers regardless of gate-to-contact spacing. Furthermore, increasing the gate-to-contact spacing results in a higher series resistance. therefore a larger spacing degrades the ESD performance for the SOI MOS devices.

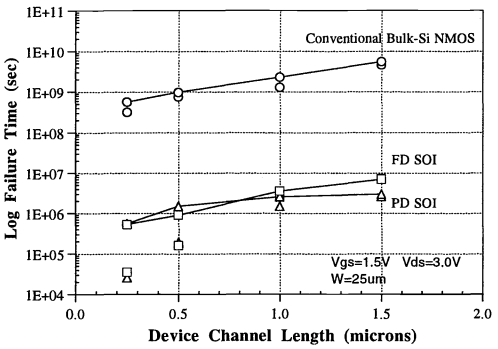

Fig. 9. Failure Time vs. Device Channel Length (Symbol: isothermal Simulation, Symbol with line: non-isothermal simulation)

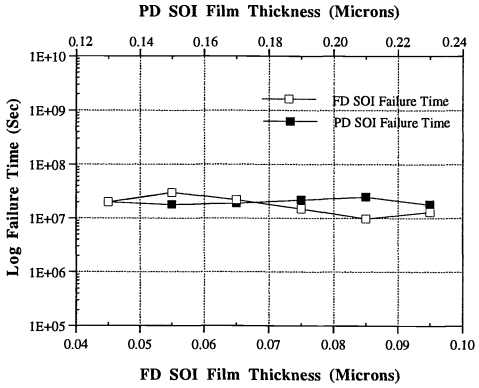

Fig. 10. SOI Device Failure Time with Silicon Film Thickness Variation

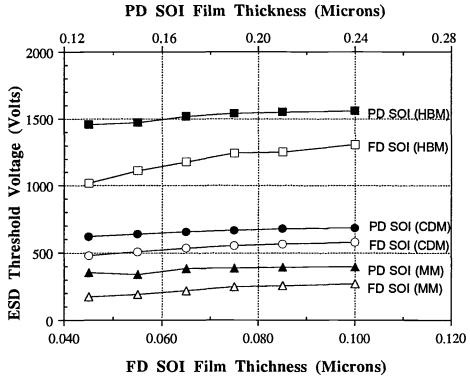

Fig. 11. SOI ESD Threshold Voltage with Silicon Film Thickness Variation for three different ESD stress (HBM, MM, CDM)

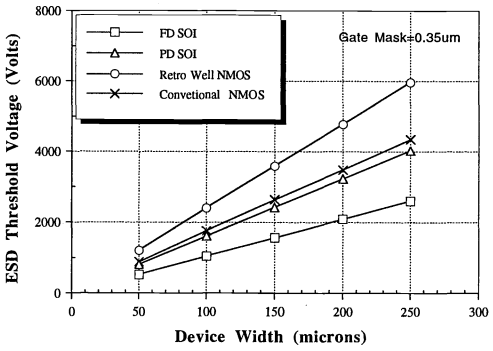

Fig. 12. Device Width vs. ESD Threshold Voltage

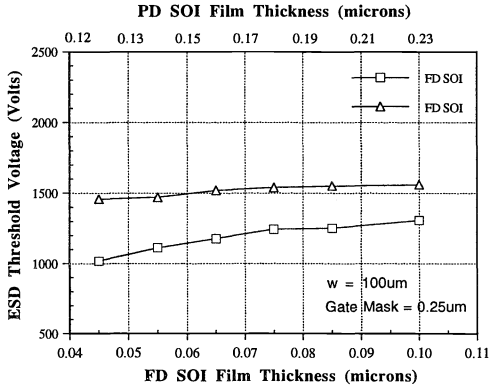

Fig. 13. SOI Silicon Film Thickness vs. Human Body Model ESD Threshold Voltage

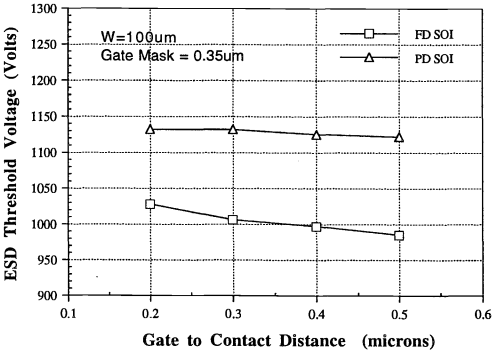

Fig. 14. Gate-to-Contact vs. Human Body Model ESD Threshold Voltage

4. EXAMPLE B: STATISTICAL ANALYSIS OF RELIABILITY

The statistical analysis scheme is shown in Figure 15. The nominal value design is setup first to examine the process flow and the corresponding device characteristics and reliability. We have chosen the 14 variables, their nominal values and manufacturing variations based on the industry data. These are shown in Table 2. When the desired output responses were obtained, the final values of the process parameters are set to the nominal values and used in the next statistical experiments. The screening design is performed to eliminate the insignificant process variables on the device reliability. A Plackett-Burman design is employed in this experiment [10]. Two output responses, ESD threshold voltage and failure time, are evaluated in the screening experiments. The statistical regression model of the device reliability will be developed in the fraction factorial experiment. The resolution IV design is employed and six target responses related to the device reliability are considered in the fractional factorial design.

In the statistical analysis, a total of 6 process input variables were identified as the important variables after the screening experiment. These are shown in Figure 16 through Figure 21. The Resolution IV design with 16 runs was employed for the fractional factorial design experiment. We have investigated total 6 output responses which are considered as an important factors for the overall device reliability.

Figures 16 and 17 show the important factors on the SOI failure time and self-heating of the FD and PD SOI devices respectively. The channel length variation due to the gate mask variation is the dominant factor on the device failure time for both PD and FD SOI device. The channel length dependance of the hot-electron injection is well known characteristics. The self-heating of the SOI device under DC stress is mostly affected by the diffusion temperatures (gate oxidation and S/D diffusion temperature). Higher gate oxidation temperature may alter channel doping and decreases the threshold voltage of the device. The channel current starts to flow even at a lower bias voltage and the self-heating is reduced. At high bias voltage, however, the self-heating is probably increased due to the current capability of the low doping channel region.

The effect of manufacturing variations on ESD protection capability of SOI technology has been studied with human body model(HBM) stress of positive polarity. The results for the ESD performance are given in Figures 18 through Figure 21. The ESD threshold voltages for the FD and PD SOI devices are controversial. The S/D diffusion temperature is the major contributor to the ESD threshold of the FD SOI, but the gate mask variation is the important factor for the PD SOI. We have conclude

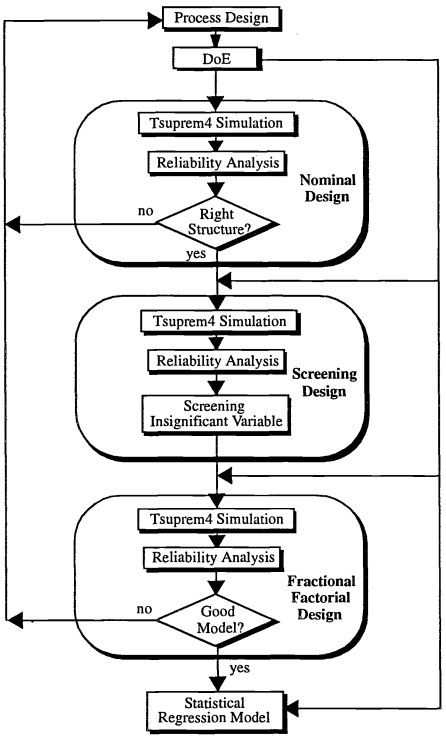

Fig. 15. Statistical Analysis Scheme

TABLE 2. SOI Process Variables and Manufacturing Variations

PROCESS VARIABLE	FD / PD SOI		
	Nominal	Variation	Units
Buried Oxide Thickness (BOT)	3800	190	A
Silicon Film Thickness (SFT)	750/ 1500*	38/ 75*	A
Silicon Film Doping (SFD)	3.0E17	1.5E16	ions/cm^3
Gate Oxidation Time (GXT)	12	1	min
Gate Oxidation Temp (GXP)	900	10	$^\circ C$
Gate Mask Variation (GMV)	-	0.00875	μm
Polygate Thickness (PGX)	0.3	0.0225	μm
Polygate Doping (PGD)	1.0E20	5.0E18	ions/cm^3
Polygate Diffusion Time (PGT)	30	1	min
Polygate Diffusion Temp (PGP)	800	10	$^\circ C$
S/D Implant Dose (SID)	2.0E15/4.0E15*	1.0E14/2.0E14*	ions/cm^2
S/D Implant Energy (SIE)	35/ 45*	1/ 1*	Kev
S/D Diffusion Time (SDT)	35/ 65*	1/ 1*	min
S/D Diffusion Temp (SDP)	900	10	$^\circ C$

* variables are used for Partially Depleted SOI process

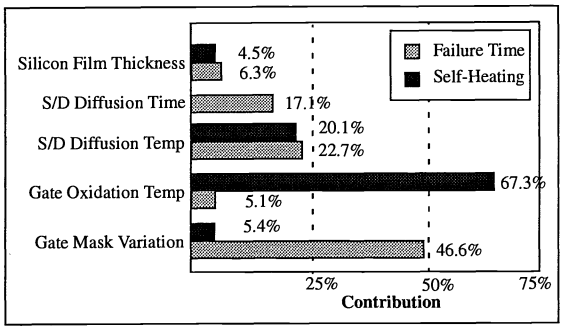

Fig. 16. Significant Factors on Failure Time & Self-Heating for FD SOII

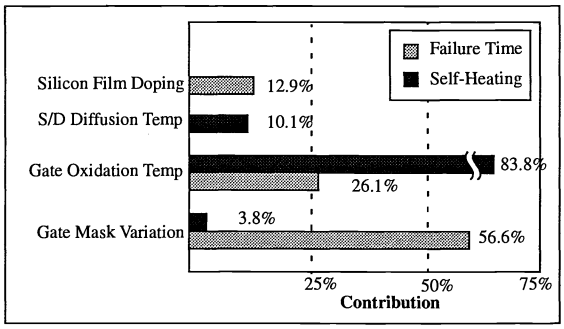

Fig. 17. Significant Factors on Failure Time & Self-Heating for PD SOI

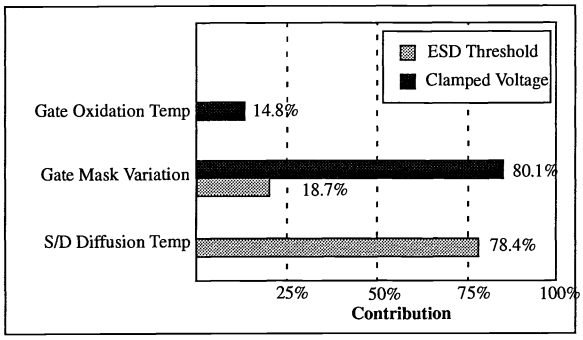

Fig. 18. Significant Factors on ESD Threshold & Clamped Voltage for FD SOI

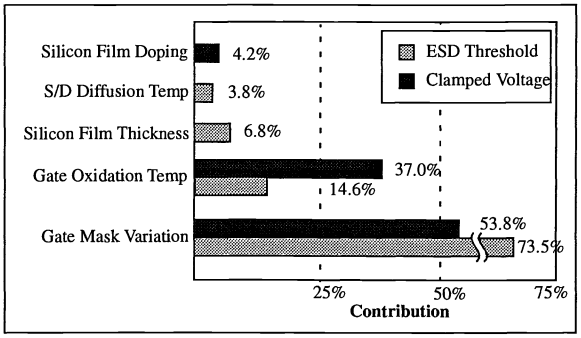

Fig. 19. Significant Factors on ESD Threshold & Clamped Voltage for PD SOI

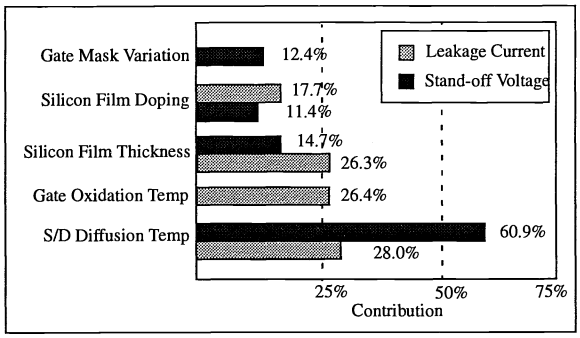

Fig. 20. Significant Factors on Leakage Current & Clamped Voltage for FD SOI

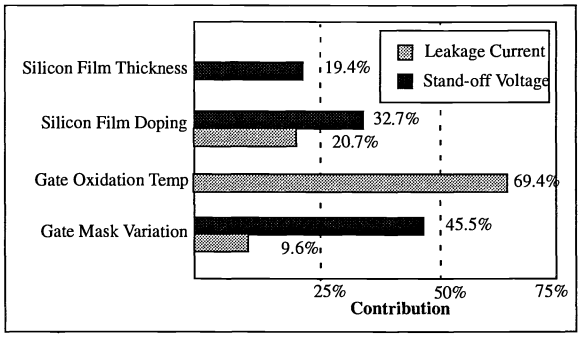

Fig. 21. Significant Factors on Leakage Current & Clamped Voltage for PD SOI

Statistical Regression Model for Device Failure Time

FD SOI Failure Time = -73226104.0 + (1.79426e+08) GMV
+ (-1.51213e+08) SFT + (-51999.2) GXP
+ (-952228) SDT+ (109730) SDP
+ (2.29542e-11) SFD ..... Eq 1

Mean: 3.8E+6 sec
Standard Deviation: 2.3E+6 sec

PD SOI Failure Time = -93505600.000000 + (-9.47624e+08) GMV
+ (553317) GXP+ (-1.91183e+08) SFT
+ (1.02458e+06) SDT + (-11762.2) SDP
+ (-2.59099e-10) SFD ..... Eq 2

Mean: 2.2E+7 sec
Standard Deviation: 1.1E+7 sec

Statistical Regression Model for ESD Threshold Voltage

FD ESD Threshold Voltage = -2783.101318 + (-3109.31) GMV
+ (1925.18) SFT + (-0.639102) GXP
+ (3.65429) SDT + (5.56948) SDP
+ (1.74101e-16) SFD ..... Eq 3

Mean: 890.5 V
Standard Deviation: 62.9 V

PD ESD Threshold Voltage = 1414.625488 + (-1049.54) GMV
+ (-0.4096) GXP + (372.161) SFT
+ (0.0522592) SDT + (0.207128) SDP
+ (8.26203e-17) SFD ..... Eq 4

Mean: 1049.1 V
Standard Deviation: 10.7 V

that the discrepancy is due to the silicon film thickness. From the result, the overall ESD performances are affected by diffusion step temperature and gate mask variation.

The prediction models shown in Eq 1-Eq 4 represent the relationship between the target responses and process input variables. The statistical information generated in this experiment can be used to provide a better understanding of the process. The important process factors identified in this analysis should be carefully controlled to improve the product consistency and reliability

5. SUMMARY AND CONCLUSION

The SOI device reliability simulator has been presented for estimating the hot-carrier induced degradation and the ESD performance. The methodology used in the simulator is to make IC's with predictable high reliability not by measuring the output at the end of production, but by controlling the process input factors that impact the product performance or reliability. The accurate failure mechanism and the statistical methodology used in the simulator allows the engineer to improve the overall reliability by reflecting the influence of the process and the layout parameters. The STADIUM SOI/Reliability software package is a useful design aid tool and the use of this tool in the device design is essential for the built-in reliability goal.

In this paper, the reliability characteristics with the process and design parameter variations and the statistical analysis of the device reliability based on the manufacturing variations have been investigated for the FD and PD SOI MOSFET's. Reasonable prediction of reliability results and statistical information have been achieved through this experiment. The self-heating effect in the SOI device improves the hot electron induced degradation even though this effect degrades the device performance. For the good ESD performance, channel length should be keep short in the SOI device. The silicon film thickness in the SOI device is one of the most important factors to be considered in the design. The thinner silicon film severely degrades the ESD performance.The provided information on the failure characteristics and on the statistical analysis can be used both for understanding the failure mechanism and for improving the reliability through design modification.

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