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Charge Injector Card for Calibration of the CMS Hadron Calorimeter

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Abstract

The Charge Injector Card simulates the response of the CMS Hadron Calorimeter (HF) sensors by injecting pulses of charge into the readout in the range of 3 fC to 330 pC.

Introduction

Particle detectors are used to observe and discover new particles. These particles are normally subatomic. The Compact Muon Solenoid (CMS) particle detector is able to detect particles that are smaller than protons. These particles are found when two protons are collided into each other; these impacts could create new particles that have never been seen before.

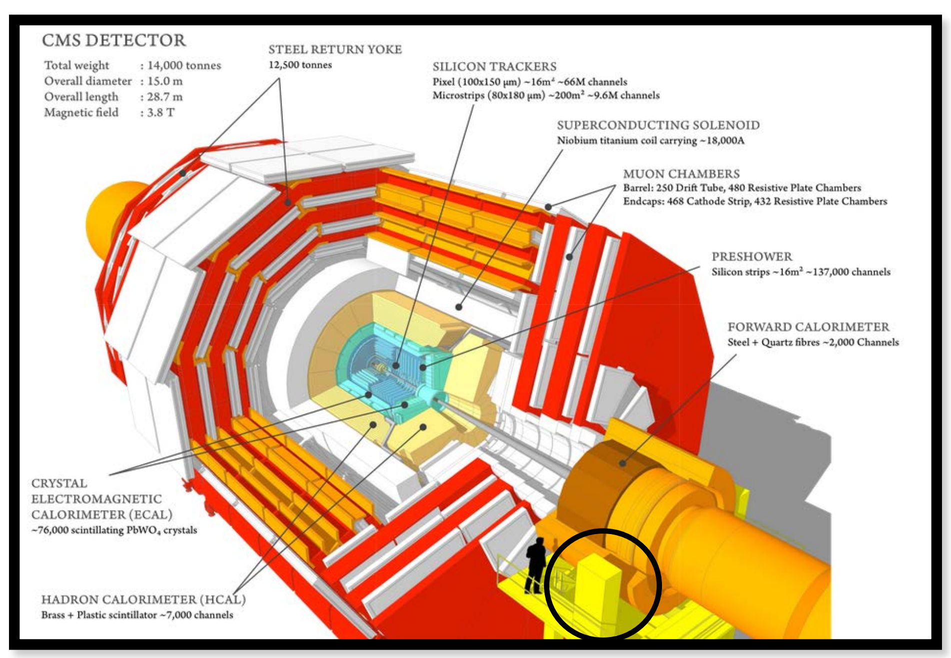

Figure 1: The CMS Detector – This is a cross section of the detector. The electronics we are testing are in the yellow section next to the silhouette.

Particle detection relies on electronic signals registered on computers. As a result, we developed a circuit board that optimized the electronic data acquisition system. This improves the range of data that can be collected by the detector. Our board calibrates the front-end readout Charge Integration and Encoding (QIE) boards that will be included in the detector. The Charge Injector Card simulates an HF response by generating pulses of charge through twelve MMCX outputs.

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Methods

- A theoretical circuit of the board was designed and simulated in CircuitLab.

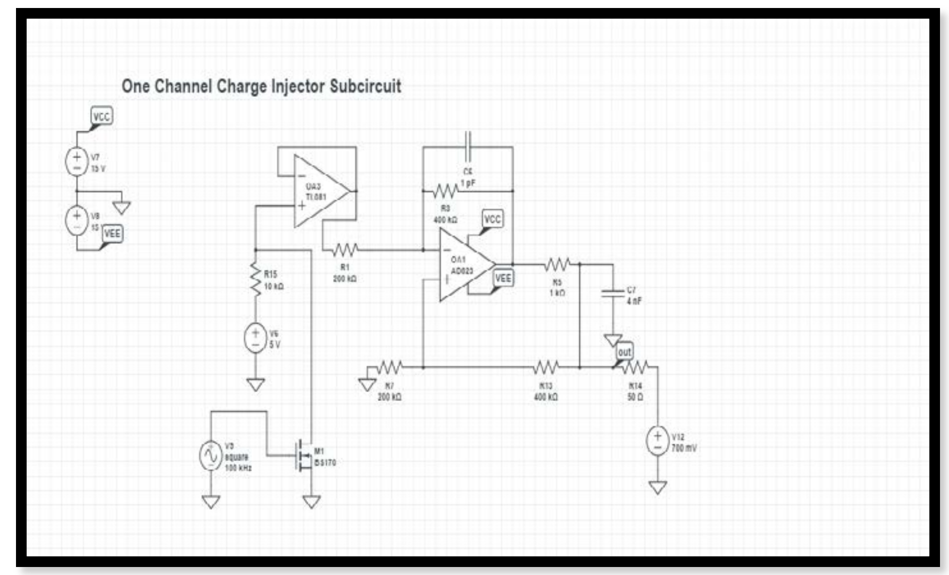
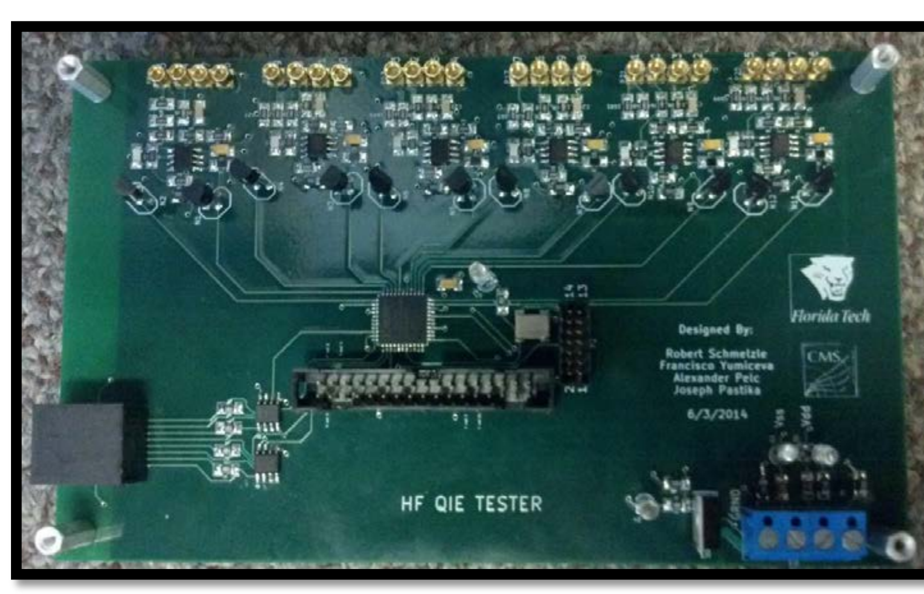


Figure 2: Schematic Sub Circuit – This is the electronic circuit schematic as seen on CircuitLab.

- The board was designed with KiCAD, a circuit board based CAD program; the sub circuit seen above was duplicated twelve times.
- The circuit board was fabricated , and all surface mount and through hole elements were soldered by hand.

Output Channels

Trigger



Power

Figure 3: The Board – The completed board with six of the twelve sub circuits visible on the top.

- Programs were written in C and a hardware description language (VHDL) that was compatible for Windows and Linux. These codes programmed a digital to analog converter (DAC) and a logic device (CPLD) respectively.
- The board was tested using power supplies, oscilloscope, and multi-meters.

Results & Conclusion

By observing the current output from the sub circuits, we determined a linear relationship between the DAC input voltage and the negative output current.

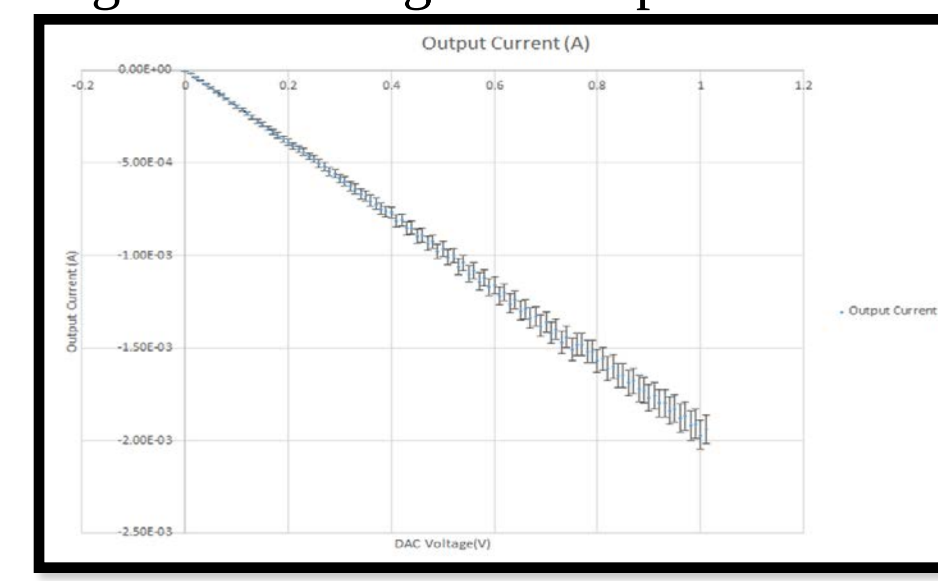


Figure 4: Output Current vs. DAC Voltage – The linear relationship with propagated error shows the proper response of the sub circuits.

The CPLD registers the rising edge of an input signal from a signal generator or an integrated oscillator and scales the signal. The negative output current seen in Figure 4 is then changed into negative output pulses by the VHDL and implementation of a transistor. Their charge was found using Ohm's Law.

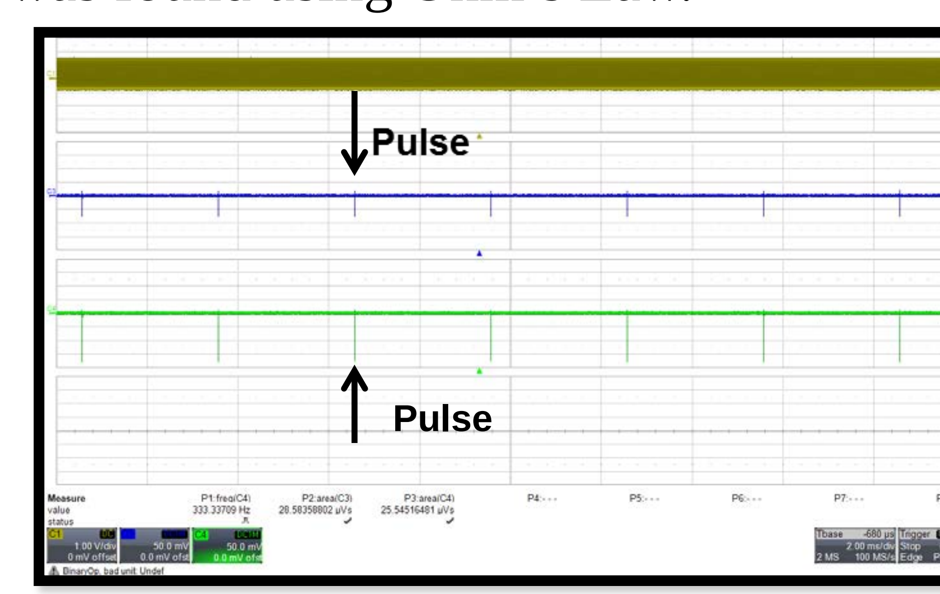


Figure 5: Output Pulses on Oscilloscope – The goal was to inject variable pulses. This is called pulse width modulation.

The yellow bar above the pulses is the input sine wave. The pulses are harmonic due to the VHDL code, and two channels' pulses differ because we programmed the DAC to output different voltages.

This result was expected. In the future, the board will perform more precise charge injections; this will improve the calibration of front-end readout QIE boards.

NORTHROP GRUMMAN

Engineering & Science Student Design Showcase at Florida Institute of Technology